The recommended CCSDS 131.2-B-1 standard introduces a Serial Concatenated Convolutional Code (SCCC). Main goal of this code is to allow an efficient use of available bandwidth, by allowing to select from 27 valid configurations with a wide range of constellations, block lengths and code rates.

The outstanding error correction performance of the SCCC code in combination with the high data rates makes this IP core an ideal fit for a variety of applications where high throughput and high spectral efficiency are keys for operation.

## Benefits

- Burst-to-burst on-the-fly configuration.
- High payload block length granularity (between 5,758 and 43,678 bits).
- High code rate granularity (code rates between 0.36 and 0.90).
- Configurable amount of turbo decoding iterations for trading-off throughput and error correction performance.
- Low-power and low-complexity design.
- Available for ASIC and FPGAs (AMD Xilinx, Intel).

## Performance Figures

- Coded throughput of up to 1.25 Gbit/s at 200 MHz and 10 iterations
- Symbol rates of up to 372 MSymbols/s at 200 MHz
- $E_S/N_0$ at 20 iterations and block error rate of $10^{-4}$:
  - $1.7dB$ (QPSK, 16,200 bits, code rate 0.52)
  - $4.01dB$ (8-PSK, 24,300 bits, code rate 0.46)
  - $8.28dB$ (16-APSK, 32,400 bits, code rate 0.59)
  - $11.56dB$ (32-APSK, 40,500 bits, code rate 0.64)
  - $14.83dB$ (64-APSK, 48,600 bits, code rate 0.69)

## Features

- Compliant with CCSDS 131.2-B-1
- Support for all 27 ACM formats
- Support for all modulation schemes (QPSK, 8-PSK, 16-APSK, 32-APSK, 64-APSK)

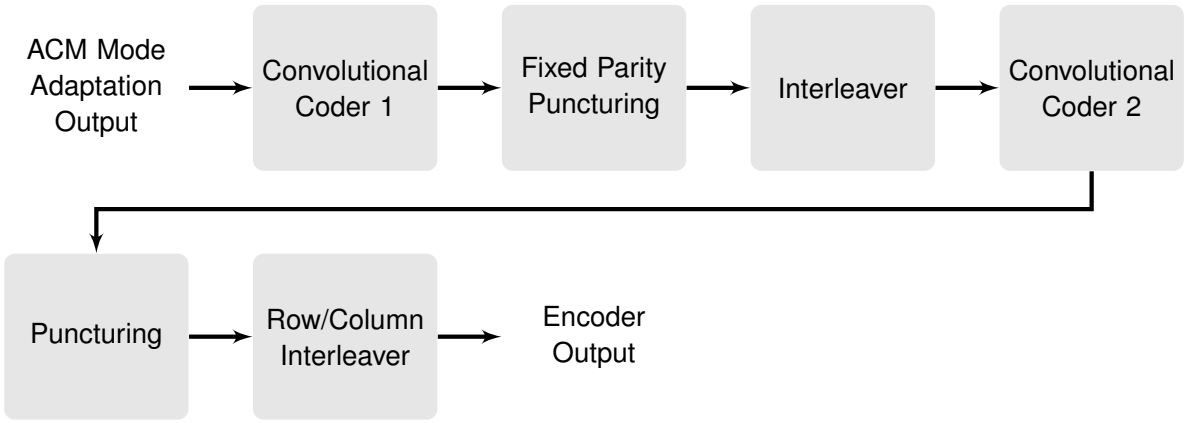
## Applications

- Satellite communication
  - High data rate telemetry applications
  - Earth Exploration Satellite Service (EESS)
- Applications with the highest demands on forward error correction
- Applications with the need for a wide range of code rates and block lengths

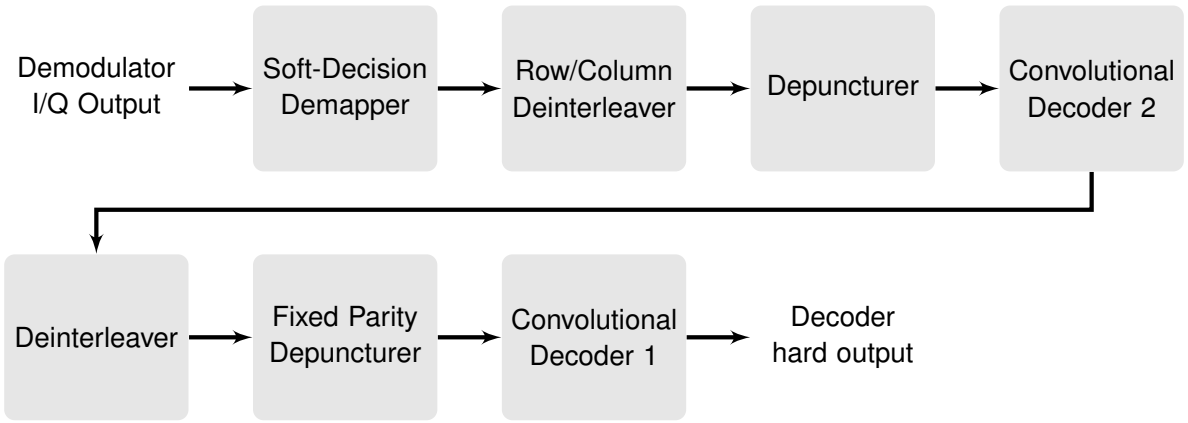
## Deliverables

- VHDL source code or synthesized netlist
- HDL simulation models e.g. for Aldec's Riviera-PRO
- VHDL testbench
- Bit-accurate Matlab, C or C++ simulation model
- Comprehensive documentation

The following figure outlines the building blocks contained within the Creonic CCSDS SCCC turbo encoder IP core.




The decoder performs the same steps on the receiver side but adds a soft-decision demapper. Decoding is an iterative process. Data is handed over multiple times between convolutional decoder 1 and 2.



## Related Products

CCSDS LDPC Encoder and Decoder

CCSDS AR4JA LDPC Encoder and Decoder

DVB-RCS2 Turbo Decoder

DVB-S2X LDPC and BCH Decoder

## About Creonic

Creonic is an ISO 9001:2015 certified provider of ready-for-use IP cores for wired, wireless, fiber, and free-space optical communications. All relevant digital signal processing algorithms are covered, including, but not limited to, forward error correction, modulation, equalization, and demodulation. The company offers the richest product portfolio in this field, covering standards like 3GPP 5G, DVB-S2X, DVB-RCS2, CCSDS, and WiFi. The products are applicable for ASIC and FPGA technologies and comply with the highest requirements with respect to quality and performance. For more information please visit our website at www.creonic.com.

## Contact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