The Creonic DVB-S2X high performance multi-carrier demodulator performs all tasks of an inner receiver while processing up to 36 carriers in parallel. The demodulator expects quantized real samples in an intermediate frequency (IF) from an analog-digital-converter (ADC). It separates the carriers with FFT/IFFT processing, and then performs all further demodulation steps in a time-multiplexed way.

It recovers timing, frequency and phase of the complex mapped symbols for each carrier individually. In addition, the core handles PL frame recovery and PL deframing.

The demodulator can work with the Creonic DVB-S2X LDPC/BCH decoder IP core by inserting a glue logic between the cores. The glue logic can be provided upon customer's request.

Benefits

- Design-time configuration of number of supported carriers (4 to 36)

- On-the-fly configuration per carrier

- Contains radio interface, carrier separation, decimator, timing recovery, equalizer, frame acquisition, and carrier recovery

- Performs and supports carrier separation, spectrum inversion, DC offset correction, I/Q imbalance correction, decimation, FFT-based blind frequency estimation, coarse frequency estimation, timing recovery, matched filtering, downsampling, frame synchronization, fine frequency correction, coarse and fine phase correction, equalization, automatic gain control, PL descrambling, and PL deframing

- AXI4-Lite memory-mapped interfaces for controlling the core and for retrieving status information

- Very fast synchronization due to different sets of filter coefficients for acquisition and tracking mode

- Configurable interrupts and output of synchronization status information

- Works with the Creonic DVB-S2X LDPC/BCH decoder

- Available for ASIC and FPGAs (AMD Xilinx, Intel on request).

Features

- Supports CCM, ACM and VCM

- Supports roll-off factors 5%, 10%, 15%, 20%, 25% to 35%

- Support for short and normal blocks (16,200 bits and 64,800 bits) with pilots only

- Support for QPSK to 256-APSK. Optional VLSNR support

- Output of XFECFRAMEs for further processing by the Creonic DVB-S2X LDPC/BCH decoder
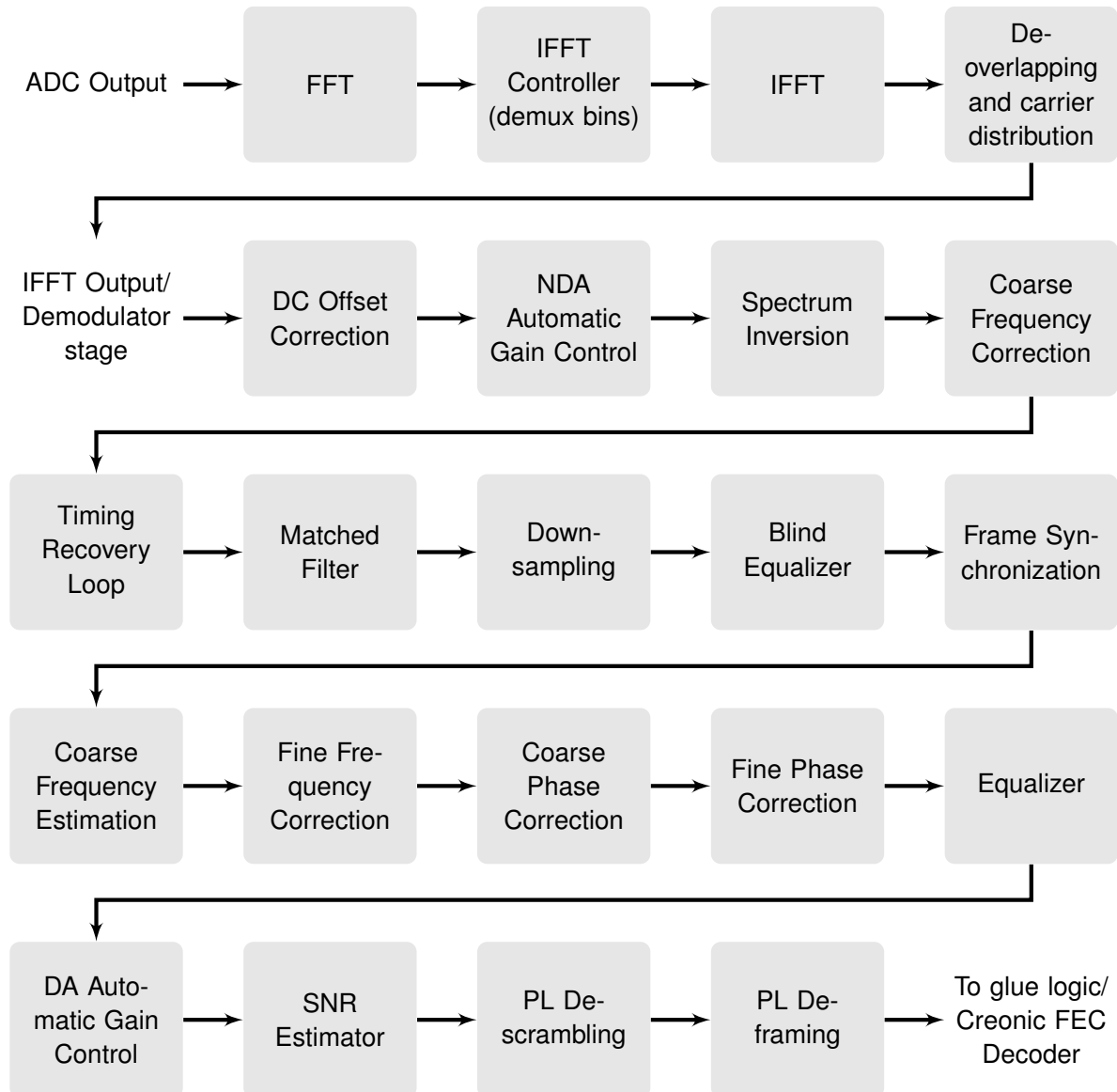
Applications

- Satellite communication
    - Digital Video Broadcasting
    - Interactive Services
    - Professional Services
    - News Gathering

Deliverables

- VHDL source code or synthesized netlist

- HDL simulation models

- C++ device driver

- Bit-accurate Matlab, C or C++ simulation model

- Comprehensive documentation

The following figure gives an overview of all components that are part of the DVB-S2X Multi-Carrier Demodulator IP core.

ADC Output → **FFT** → **IFFT Controller (demux bins)** → **IFFT** → **De-overlapping and carrier distribution**

IFFT Output/ Demodulator stage → **DC Offset Correction** → **NDA Automatic Gain Control** → **Spectrum Inversion** → **Coarse Frequency Correction**

Timing Recovery Loop → **Matched Filter** → **Down-sampling** → **Blind Equalizer** → **Frame Synchronization**

Coarse Frequency Estimation → **Fine Frequency Correction** → **Coarse Phase Correction** → **Fine Phase Correction** → **Equalizer**

DA Automatic Gain Control → **SNR Estimator** → **PL De-scrambling** → **PL De-framing** → To glue logic/ Creonic FEC Decoder

Related Products

[DVB-S2X LDPC/BCH Decoder](#)

[DVB-S2X Modulator](#)

[DVB-S2X Demodulator](#)

[DVB-GSE Encapsulator and Decapsulator](#)

[NCR Processor](#)

About Creonic

Creonic is an ISO 9001:2015 certified provider of ready-for-use IP cores for wired, wireless, fiber, and free-space optical communications. All relevant digital signal processing algorithms are covered, including, but not limited to, forward error correction, modulation, equalization, and demodulation. The company offers the richest product portfolio in this field, covering standards like 3GPP 5G, DVB-S2X, DVB-RCS2, CCSDS, and WiFi. The products are applicable for ASIC and FPGA technologies and comply with the highest requirements with respect to quality and performance. For more information please visit our website at www.creonic.com.

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