Creonic provides the following field-proven IP cores:

- DVB-S2X Modulator M100 / M400
- DVB-S2X Demodulator
- DVB-S2X LDPC/BCH Decoder

## DVB-S2X Modulator M100 / M400

The Creonic DVB-S2X high performance modulator performs all tasks of an inner transmitter. The modulator expects BBFrames after mode adaptation as input and performs stream adaptation, FEC encoding, mapping, PL framing and modulation. In addition, the core can perform baseband interpolation and output gain adjustment. The output of the core is designed to be followed by a DAC and RF front end.

## Benefits

- Validated against the field-proven Creonic DVB-S2X demodulator and decoder IP cores.
- Easy-to-use mode adaptation input interface.
- Provides interpolated and gain-adjusted ZF baseband signal.
- The modulator contains padder, frame CRC computation, BB scrambler, BCH encoder, LDPC encoder, bit interleaver, optional VLSNR processor, bit mapper, dummy PL frame insertion, PL signaling, pilot insertion, PL scrambler, baseband filter, integer interpolator, fractional interpolator (M100 only), and gain adjustment.
- Can be complemented with the Creonic DVB-CID modulator.
- Low-power and low-complexity design.
- AXI4-Lite interface for controlling and retrieving status information.
- Flexible output interface, which can be driven by an external clock for easy synchronization with DAC.
- Available for ASIC and FPGAs (AMD Xilinx, Intel, Microchip).

## Features

- Compliant with DVB-S2 and DVB-S2X
- Supports ACM, CCM, and VCM modes
- Support for short and normal frames (16,200 bits and 64,800 bits)
- Support for QPSK to 256-APSK
- Support for very low SNR modes (VLSNR) optional

## Applications

- Satellite communication
  - Digital Video Broadcasting
  - Interactive Services
  - Professional Services
  - News Gathering

## Deliverables

- VHDL source code or synthesized netlist
- HDL simulation models
- Bit-accurate Matlab, C or C++ simulation model
- Comprehensive documentation

## Key Features

- M100: Symbol rate of up to 200 MSymbols/s for all modes.
- M400: Symbol rate of up to 400 MSymbols/s for all modes.

The following figure gives an overview of all components that are part of the DVB-S2X Modulator IP core.

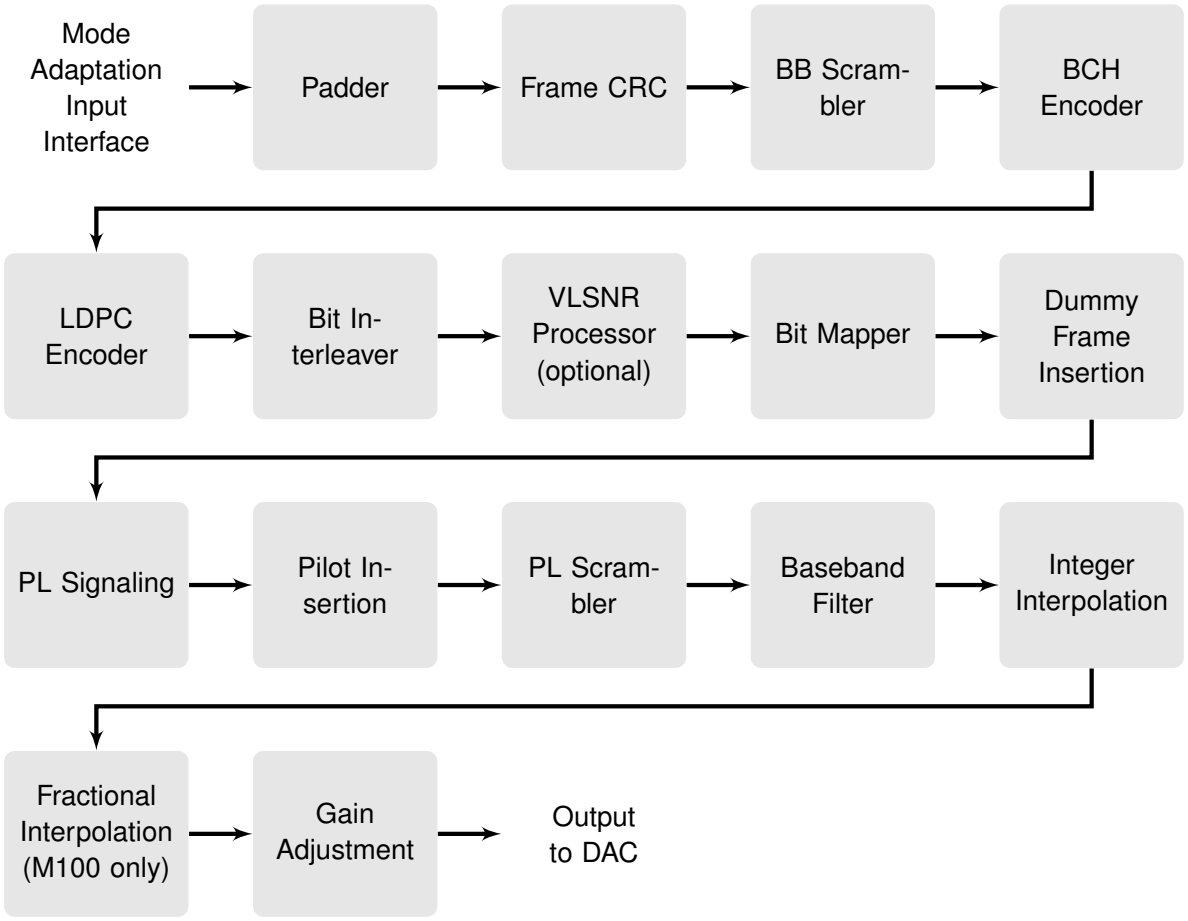



**Figure 0.1:** Creonic DVB-S2X Modulator IP building blocks.

## DVB-S2X Demodulator

The Creonic DVB-S2X high performance demodulator performs all tasks of an inner receiver. The demodulator expects the quantized, complex baseband samples from an analog-digital-converter (ADC) and recovers timing, frequency and phase of the complex mapped symbols. In addition, the core handles PL frame recovery and PL de-framing. The demodulator's output perfectly fits the Creonic DVB-S2X forward error correction IP core that implements LDPC and BCH decoding.

## Benefits

- Validated against 3rd party DVB-S2X modulators.
- Contains radio interface, decimator, timing recovery, equalizer, frame acquisition, and carrier recovery.
- Performs and supports spectrum inversion, DC offset correction, I/Q imbalance correction, decimation, coarse frequency estimation, timing recovery, matched filtering, downsampling, frame synchronization, PL descrambling, fine frequency correction, phase correction, automatic gain control, and PL deframing.
- Low-power and low-complexity design.
- On-the-fly configuration.
- AXI4-Lite interface for controlling the core and retrieving status information.
- Very fast synchronization due to different sets of filter coefficients for acquisition and tracking modes.
- Configurable interrupts and output of synchronization status information.
- Perfectly fits to the Creonic DVB-S2X LDPC/BCH decoder.
- Available for ASIC and FPGAs (AMD Xilinx, Intel).

## Features

- Compliant with DVB-S2 and DVB-S2X
- Supports ACM, CCM, and VCM modes
- Support for short and long blocks (16,200 bits and 64,800 bits)
- Support for QPSK to 256-APSK
- Support for very low SNR modes (VLSNR) optional
- Output of XFECFRAMEs for further processing by the Creonic FEC decoder

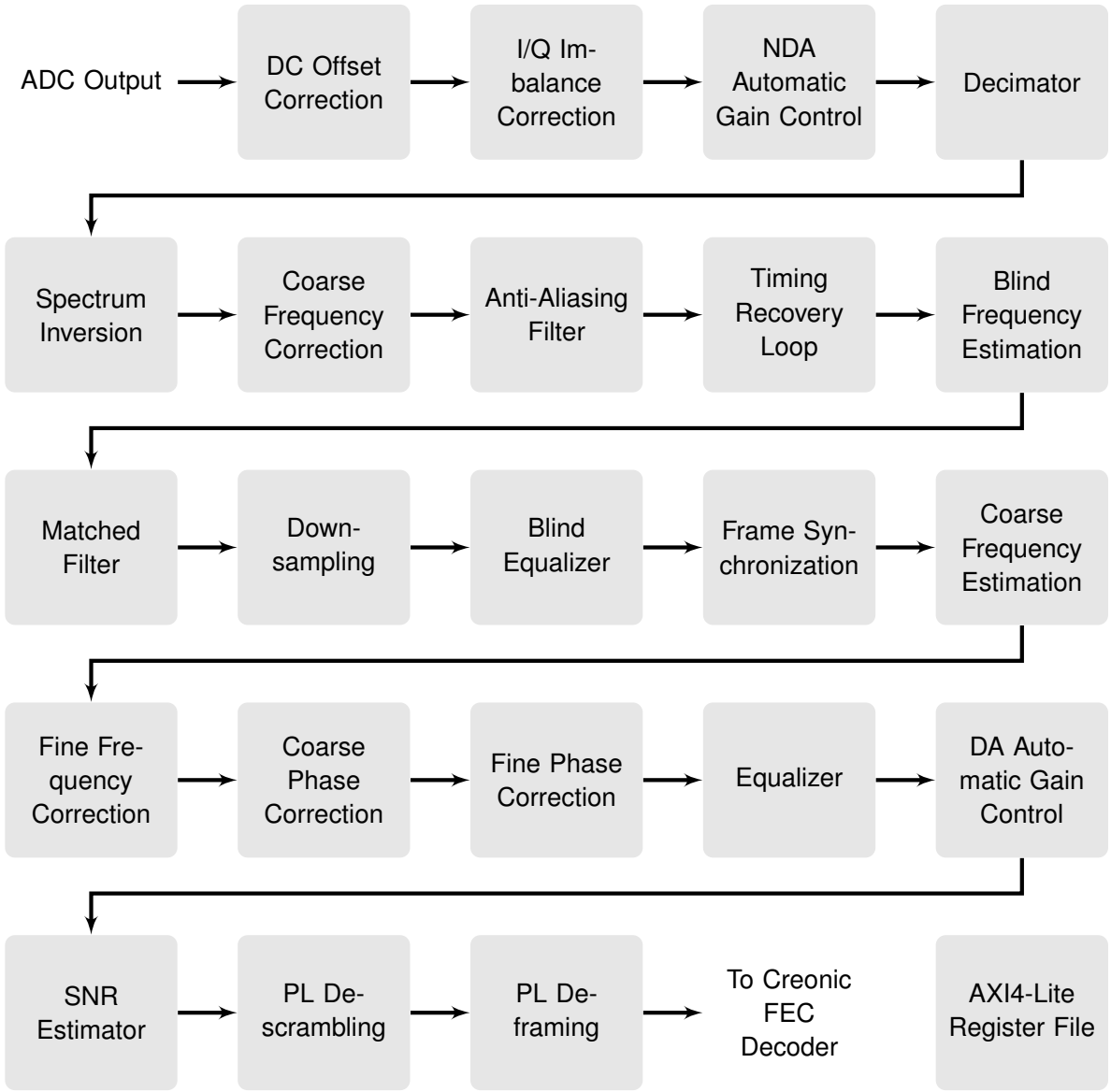
## Applications

- Satellite communication
  - Digital Video Broadcasting
  - Interactive Services
  - Professional Services
  - News Gathering

## Deliverables

- VHDL source code or synthesized netlist
- HDL simulation models
- Bit-accurate Matlab, C or C++ simulation model
- Comprehensive documentation

The following figure gives an overview of all components that are part of the DVB-S2X Demodulator IP core:



## DVB-S2X LDPC/BCH Decoder

The Creonic DVB-S2X decoder is a silicon-proven, scalable solution that allows for symbol rates of up to 100 MSymbols/s on state-of-the-art FPGAs.

## Benefits

- Validated against 3rd party DVB-S2X modulators.
- Silicon-proven IP core.
- Based on industry-proven design for DVB-S2.
- Soft-Decision demapper, block deinterleaver, LDPC decoder, BCH decoder, descrambler, and CRC checks included.
- Low-power and low-complexity design.
- Frame-to-frame on-the-fly configuration.
- Design-time configuration of throughput for optimal resource utilization.
- Faster convergence due to layered LDPC decoder architecture.
- Early stopping criterion for iterative LDPC decoder, saving a considerable amount of energy.
- Configurable amount of LDPC decoding iterations for trading-off throughput and error correction performance with on-the-fly selection in ACM/VCM modes.
- Collection of statistics (error rates, average number of iterations, signal-to-noise ratio (SNR)).
- Available for ASIC and FPGAs (AMD Xilinx, Intel).

## Key Features

- Signal-to-noise ratio ranges from -9.6 to 19.8 dB.
- Throughput of 100 MSymbols/s or above for all modes.

## Features

- Compliant with DVB-S2 and DVB-S2X
- Support for decoding of BBFRAMEs
- Support for ACM, CCM, and VCM
- Support for very low SNR modes (VLSNR) with SNRs below -9 dB.
- Support for short, medium, and normal frames (16,200 bits, 32,400 and 64,800 bits)
- Support for BPSK, QPSK, 8-PSK, 16-APSK, 32-APSK, 64-APSK, 128-APSK, and 256-APSK

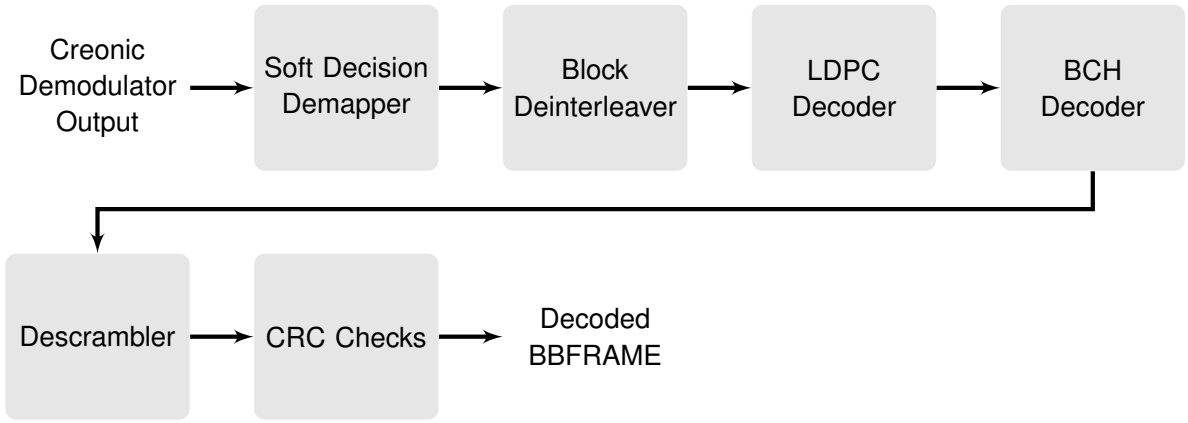
## Applications

- Satellite communication
- Applications with the highest demands on forward error correction
- Applications with the need for a wide range of code rates (1/10 to 9/10)

## Deliverables

- VHDL source code or netlist
- HDL simulation models
- VHDL or SystemC testbench
- Bit-accurate Matlab, C or C++ simulation model
- Comprehensive documentation

The following figure gives an overview of all components that are part of the DVB-S2X LDPC/BCH decoder IP core:




## Related Products

DVB-GSE Encapsulator and Decapsulator

DVB-S2X Wideband Modulator

DVB-S2X Wideband Demodulator

DVB-S2X Wideband Decoder

DVB-S2 LDPC and BCH Decoder

DVB-CID Modulator

## About Creonic

Creonic is an ISO 9001:2015 certified provider of ready-for-use IP cores for wired, wireless, fiber, and free-space optical communications. All relevant digital signal processing algorithms are covered, including, but not limited to, forward error correction, modulation, equalization, and demodulation. The company offers the richest product portfolio in this field, covering standards like 3GPP 5G, DVB-S2X, DVB-RCS2, CCSDS, and WiFi. The products are applicable for ASIC and FPGA technologies and comply with the highest requirements with respect to quality and performance. For more information please visit our website at www.creonic.com.

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