DVB-S2 (Digital Video Broadcast - Satellite 2nd Generation) is an ETSI standard of the second generation for digital data transmission via satellites. It was published in 2005, being the first standard of the second generation DVB standards (DVB-S2/-T2/-C2). Because of its capacity-approaching forward error correction, today DVB-S2 is the de-facto standard in satellite communication and other applications. The Creonic DVB-S2 IP core integrates the forward error correction as defined by the standard (including LDPC and BCH decoder).

DVB-S2 Decoder

The Creonic DVB-S2 LDPC and BCH decoder IP core performs forward error correction as defined within the standard. Furthermore, it includes additional signal processing before and after forward error correction (soft-decision demapping, deinterleaving, descrambling). Key features of the decoder are:

- Soft-Decision demapper, block deinterleaver, LDPC decoder, BCH decoder, descrambler, and CRC check included.

- Low-power and low-complexity design.

- Frame-to-frame on-the-fly configuration.

- AXI4-Stream handshaking interfaces for seamless integration.

- Design-time configuration of throughput for optimal resource utilization.

- Faster convergence due to layered LDPC decoder architecture.

- Early stopping criterion for iterative LDPC decoder, saving a considerable amount of energy.

- Configurable amount of LDPC decoding iterations for trading-off throughput and error correction performance.

- Collection of statistic information (number of modified bits, number of iterations, decode success).

- Available for ASIC and FPGAs (AMD Xilinx, Intel).

Features

- Compliant with ETSI EN 302 307 V1.2.1 (2009-08) (DVB-S2)

- Supports ACM, CCM, and VCM modes

- Support for decoding of BBFrames

- Support for short and long blocks (16,200 bits and 64,800 bits)

- Support for all modulation schemes (QPSK, 8-PSK, 16-APSK, and 32-APSK)

- Support for all interleaving schemes of all modulation schemes

- Support for all LDPC and BCH codes as defined by the standard

Applications

- Satellite communication
  - Digital Video Broadcasting
  - Interactive Services
  - Professional Services
  - News Gathering

- Applications with the highest demands on forward error correction

- Applications with the need for a wide range of code rates (1/5 to 9/10)

DVB-S2 Encoder

The Creonic DVB-S2 LDPC and BCH encoder IP core performs encoding for forward error correction as defined within the standard, and furthermore includes additional signal processing before and after encoding, i.e., interleaving and descrambling. Key features of the encoder are:

- Scrambler, BCH encoder, LDPC encoder, and block interleaver included.

- Low-power and low-complexity design.

- Frame-to-frame on-the-fly configuration.

- AXI4-Stream handshaking interfaces for seamless integration.

- Design-time configuration of throughput for optimal resource utilization.

- Available for ASIC and FPGAs (AMD Xilinx, Intel, Microchip).

Deliverables

- VHDL source code or synthesized netlist

- HDL simulation models e.g. for Aldec's Riviera-PRO

- VHDL testbench

- Bit-accurate Matlab, C or C++ simulation model

- Comprehensive documentation

Related Products

[DVB-GSE Encapsulator and Decapsulator](#)

[DVB-S2/DVB-S2X Modulator](#)

[DVB-S2/DVB-S2X Demodulator](#)

[DVB-S2X Decoder](#)

[DVB-RCS2 Turbo Decoder](#)

About Creonic

Creonic is an ISO 9001:2015 certified provider of ready-for-use IP cores for wired, wireless, fiber, and free-space optical communications. All relevant digital signal processing algorithms are covered, including, but not limited to, forward error correction, modulation, equalization, and demodulation. The company offers the richest product portfolio in this field, covering standards like 3GPP 5G, DVB-S2X, DVB-RCS2, CCSDS, and WiFi. The products are applicable for ASIC and FPGA technologies and comply with the highest requirements with respect to quality and performance. For more information please visit our website at www.creonic.com.

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